A Highly Efficient Noise Suppression Technique for Si-based RFIC

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ABSTRACT — **A highly efficient CMOS process technique of suppressing the transmission of high-frequency noise induced by fast-switching MOS gates and/or spiral inductors through silicon substrate has been attained. The isolated n^+-pocket structure designed in this work has proven to be very effective in guarding vulnerable devices from remnant high-frequency noise roaming in the substrate. The protecting structures shall become a decisive measure in future success of Si-based RFIC applications.**

I. INTRODUCTION

With significant advancement of CMOS technologies and the merit of low cost, silicon-based RFICs and RF embedded system on chip (SOC) have emerged as desirable complete solution to satisfy the rapidly growing demand of wireless communication applications [1]. The wireless communication system based on silicon technology will accommodate more functions as a result of high circuit integration density. However, the ultimate goal of constructing analog and digital circuits all together on a single chip has been hindered by the lossy nature of silicon substrate.

The major challenge arises from the simultaneous switching of MOSFETs. At low operating frequencies, the substrate impedance is sufficient to block the switching noise. As the clock rate approaches 1 GHz and beyond, the problem of injected noise that would transmit through a common silicon substrate and jeopardize neighboring devices becomes serious [2]. Although much effort has been made in reducing substrate noise [3][4], most techniques fail to sustain efficient isolation characteristics as frequency approaches GHz range. It is therefore necessary to develop techniques that can put a stop to the injected noise from MOS-gate switching and retain the performance of passive elements. In this paper, we demonstrate a promising technique to construct isolated n^+-pocket structures for RF substrate noise isolation in silicon-based RFICs. As shown in Fig. 1, the noise-injecting terminals and vulnerable devices would be surrounded by isolated pocket structure while passive elements like spiral inductors would be left unbound. Under such arrangement, a highly efficient way to drain out substrate noise can be expected.

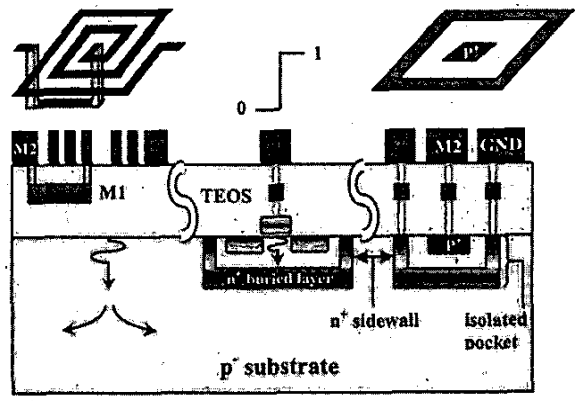

Fig. 1. A schematic that illustrates the mechanism of substrate-noise generation and suppression.

II. EXPERIMENTAL

To protect vulnerable devices on wafer from the disturbance of substrate noise, isolated high-dose n^+-pocket structures are constructed under the following sequence. A (100) p-type starting wafer was first heavily implanted with arsenic, then a 1.0-μm-thick p^--epi layer was grown and a buried n^+ layer was created. To carry on, allocated N-wells were implanted with phosphorus and followed by standard MOSFET and p^+ contact process within the areas. As the N-wells diffused downward during thermal process and merged with the buried n^+ layer, several n^+-pocket structures were then formed. Notice that for sidewall configuration, phosphorus was chosen so that the sidewalls would reach the buried layer. On the other hand, arsenic was chosen as buried layer for its slower diffusion that would prevent buried-layer-width spreading and concentration lowering during subsequent thermal cycles. For isolation efficiency comparison, some test wafers employed blanket buried layer while others contained patterned buried layer. Fig. 2 shows the cross-sectional SEM picture of a complete pocket structure. In order to derive the quantitative relationship between structure variation and its efficiency in suppressing substrate noise, forward transmission coefficient (s_{21}) is measured by HP8510C (network analyzer).

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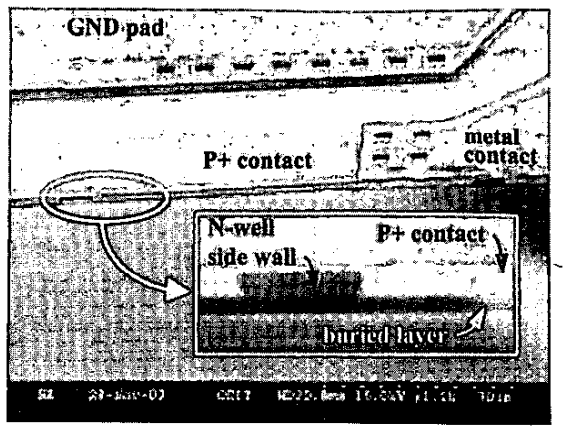

Fig. 2. A cross section SEM picture of the n^+-pocket structure with p^+ contact enclosed.

III. Results And Discussion

The experimental results of the test keys with different isolation approaches including p^+ guard rings and pocket structures are shown in Fig. 3 & 4. Notice that only the data of test structures with p^+ substrate contacts on both transmitting and receiving terminals are shown. For the cases of MOS gates as transmitting terminals, the transmission ratios of test keys with pocket structures tend to reach the detection limit of characterization system and cause ambiguity in data analysis. In addition, minimum distance between noise-injecting terminal and receiving terminal (21 μm) has been adopted to prevent hitting the detection limit.

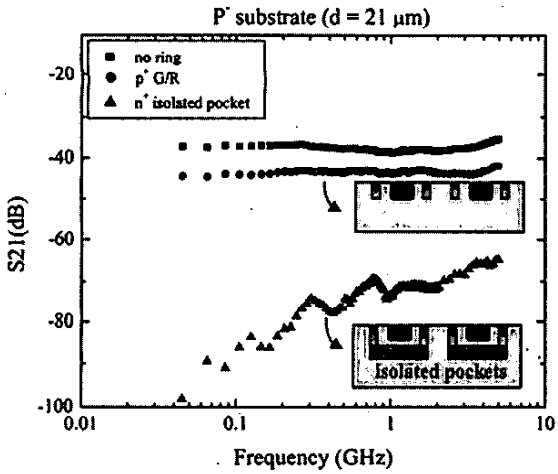

Fig. 3. Test keys with isolated n^+ pocket structures exhibit superior substrate noise suppression efficiency over p^+ guard rings.

In Fig. 3, the noise transmission coefficient s_{21} of test keys with p^+ guard rings only exhibits some degree of improvement compared to the ones without any protection measure due to the awfully short distance between noise-injecting and receiving terminals. With isolated n^+-pocket structures, the noise transmission ratio is reduced significantly and s_{21} as low as –75dB at 1GHz has been obtained. The dramatic improvement of n^+-isolated pocket structures over p^+ guard rings to suppress substrate noise can be attributed to the tight-enclosing nature and the high dosage of pocket structures. The conductive n^+ layer that surrounds MOSFETs and p^+ contacts would basically absorb most of the noise and drain it out of the substrate. The ground to which pocket structures are connected serves as the final sink for all of the noise. However, if the buried n^+ layer extends and connects different pocket structures as the case of blanket buried layer, a serious deterioration of noise suppression characteristics would result as shown in Fig. 4. For those "connected" pocket structures, the blanket n^+-buried layer serves as a superfluous conducting path for high-frequency noise to travel along and arrives at the receiving terminals. The n^+-buried layer does the same harm even for the test structures with or without guard rings. At low frequencies, the n^+-buried layer prevents the noise from going down the substrate and thus effectively reduces the transmission channel width of substrate noise. As frequency increases, the obstructed signal finds a convenient ride to travel in the substrate. Therefore, serious noise spreading at high frequencies has been observed for the cases with and without p^+ guard rings as long as the buried layer is present.

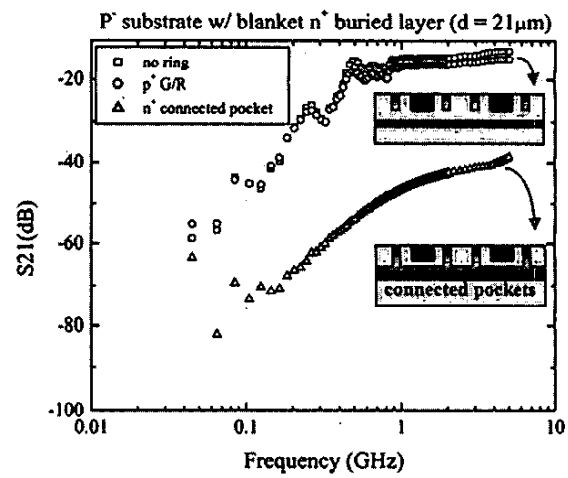

Fig. 4. Test keys with blanket n^+ buried layer exhibit deteriorated noise suppression efficiency compared to their counterparts for all cases.

Various fabrication procedures can be used to form pocket structures. Previous works have demonstrated that a deep N-well (DNW) formed by high-energy implant of phosphorous in conjunction with sidewall N-well can also create pocket structures. The process of deep implant is relatively easier as long as the high-energy (MeV) implanter is available. However, the constraint of deep-implant process is the doping concentration. Should a deep implantation with high doping level be conducted, it would cause serious crystal damage and hence not used in standard CMOS process. As a result, only low-level or moderate-level doping is allowed for deep-implant process. Fig. 5 compares the noise suppression characteristics between pocket structures with different fabrication procedure and doping conditions. The main difference lies in the forming procedure of buried layer. A buried layer formed by surface implantation allows arbitrary choice of doping level while deep implantation only allows lower doping level. In the case of sidewall implantation, there is no particular limitation of doping level if only the dopants can join the buried layer when thermal process is finished. Experimental results show that the pocket structures with surface implantation (doping level = $2x10^{19}$ cm^{-3}) exhibit superior characteristics of noise immunity than the ones with deep implantation. The pocket structures with deep implantation by To, *et. al.* in 2001 IEDM [5] and our previous work (doping level = $2x10^{17}$ cm^{-3}) [6] suffers higher noise penetration rate at GHz-frequency range due to lower concentration of buried layer by process limitation. It is therefore clear to see that the doping concentration of buried layer plays a critical role in determining the noise suppression capability.

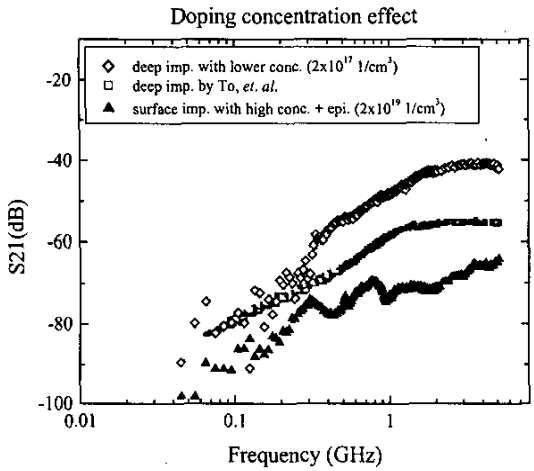

Fig. 5. The impact of doping concentration and pocket fabrication process on substrate noise suppression efficiency.

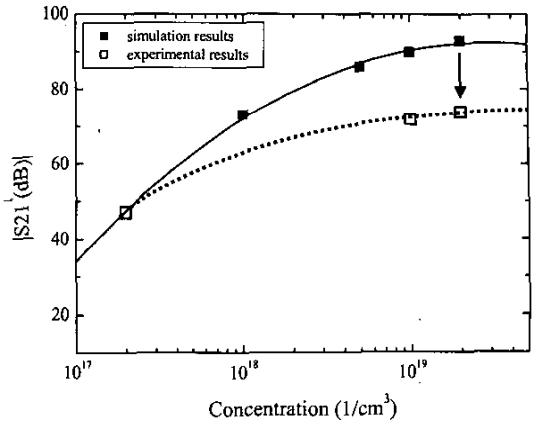

Fig. 6. Experimental data and simulation results of noise suppression characteristics with various doping concentration of n^+-pocket structures are compared.

Although the isolated n^+-pocket structures exhibit significant improvement on substrate-noise suppressing capability, experimental results do not match too well with simulation under high-doping concentration condition. The commercial device simulation tool "Atlas" by SILVACO has been used in this work to predict the noise-coupling characteristics of various test structures and the comparison between experimental data and simulation results for n^+-pocket structures is displayed in Fig. 6. The predicted results by simulation indicate that an extremely low noise transmission ratio (–92dB) at 1 GHz should be obtained with doping level of n^+-pocket structure to be $2x10^{19}$ cm^{-3}. However, measured data shows –75dB at 1 GHz in reality. The reason for the deviation can be resolved by SRP (Spreading Resistance Profiling) measurement. An SRP system detects electrically active dopant concentration in silicon by measuring spreading resistivity profile of the sample and converts it to dopant concentration. As shown in Fig. 7, the phosphorus concentration in the sidewall (~$2x10^{17}$ cm^{-3}) is much lower than expected. The concentration lowering in the sidewall is believed to be the result of the fast diffusion of phosphorus during thermal process. In the simulation, uniform doping level around sidewalls and buried layer is expected. In practical process, however, the phosphorus concentration drops below the doping level of n^+-buried layer too much and thus becomes a weak defense line in the pocket structures. One possible solution for this problem is to replace phosphorus with arsenic in the sidewall implantation. However, a more complex process will be required in order to construct sidewalls that possess enough depth to connect the n^+-buried layer and form isolated n^+-pocket structures.

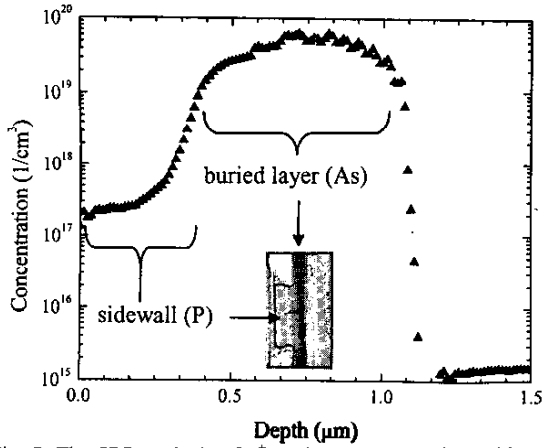

Fig. 7. The SRP analysis of n^+-pocket structures along sidewall shows the active dopant concentration profile.

Although pocket structures are very effective in substrate noise isolation, they are harmful to spiral inductors as p^+ guard rings do. Fig. 8 shows that the maximum Q value of a spiral inductor is reduced significantly (20%) if a p^+ guard ring is constructed underneath. The reason for the significant Q-value reduction is that the conductive n^+ layer allows strong eddy current to be induced and hence drains out the magnetic energy from the inductors. Fortunately, the dilemma can be worked out by constructing the isolated pocket structures only around the active devices to be isolated. The magnetic energy loss of inductors would be negligible as long as the pocket structures are kept far away.

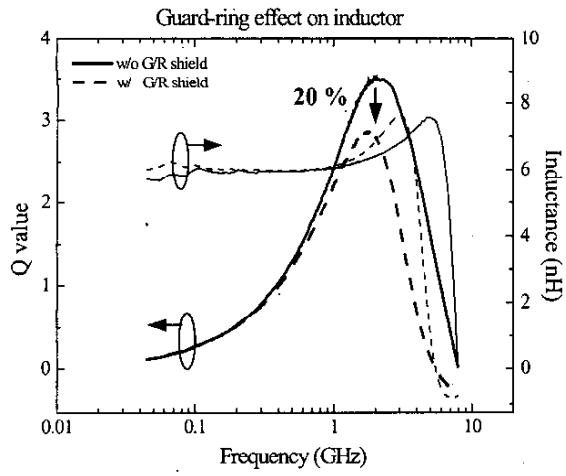

Fig. 8. The influence of substrate noise suppression structures on spiral inductors is to reduce their Q values.

IV. Conclusion

A highly efficient structure to suppress substrate noise for future RFIC design has been demonstrated. Among all isolation structures, highly doped n^+-pocket structures exhibits the best performance in noise suppression at high frequencies. The major improvement of noise isolation effect comes from the identification of the key factor and the proper choice of applicable process. From the results above, one could determine proper isolation conditions for best noise suppression in RFIC applications.

Acknowledgement

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